

SRAM IMC without the usual limitations

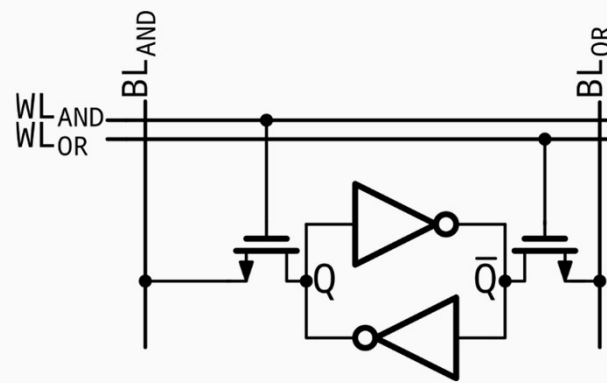
Performance gains with lower area overhead and stability advantages compared to conventional SRAM IMC

STATUS QUO

Boolean SRAM in-memory computing (IMC) is an important component of current research, such as hardware-based neural networks and edge computing. In conventional approaches, several cells are usually evaluated simultaneously via the same bit lines to implement the AND and OR functions. However, this causes difficulties in maintaining the stored value during a read operation and requires larger cell layouts due to necessary adjustments.

OUR TECHNOLOGY

In contrast to conventional IMC, our implementation executes Boolean instructions during a write access. To do this, an external operand (which can also be read from the SRAM beforehand) is applied to the bit lines and only WL_{AND} is activated for the AND instruction, or only WL_{OR} for the OR instruction. For conventional setting, both word lines are activated. After the instruction, the result is automatically stored in the activated SRAM cell and therefore does not need to be written back as is usually the case.



BENEFITS

- Performance gains through IMC
- Stability advantages and space savings compared to conventional SRAM IMC
- No need for write-back

APPLICATION POSSIBILITIES

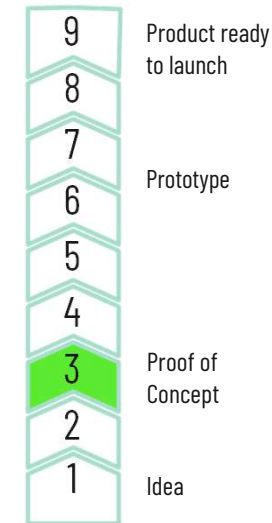
Important areas of application include the design of data-intensive computer architectures such as:

- Hardware-based neural networks in SRAM
- Highly parallel computing
- But also as a smart cache for conventional computer architectures

COMMERCIALIZATION OPPORTUNITIES

There are various possibilities for cooperation between the industrial partner and TU Darmstadt: from an exchange with the know-how carriers of the technology up to a close cooperation in case of further development needs. The technology is protected by intellectual property rights and can be used by the industry partner after a sale or licensing agreement.

CURRENT STAGE OF DEVELOPMENT TECHNOLOGY READINESS LEVEL (TRL)



Development is at level 3: The new SRAM architecture has been positively evaluated in Monte Carlo simulations. An initial test chip is being developed.

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